

REMARKS

In the outstanding non-Final Official Action, claims 1-3 were rejected under 35 U.S.C. §102(e) as being anticipated by Shinkai, with claims 1 and 2 being rejected under 35 U.S.C. §102(e) as being anticipated by Asghar or Yamada et al, and claim 1 additionally being rejected under 35 U.S.C. §102(b) as being anticipated by Guttag et al, all for the reasons of record.

In response, claim 1 is herewith amended in order to add substantial additional structural features as shown and described in the instant application, without adding any new matter. More particularly, claim 1, as herein recommended now more particularly and precisely recites that the invention additionally comprises a computer having a direct connection to the command decoder, with a common bus having input and output connections, and with the computer, the command decoder and the memory all being directly connected to the common bus.

It is respectfully submitted that the present invention, as now more specifically recited, is neither shown nor suggested by the cited and applied references. Accordingly, allowance of the instant application is respectfully submitted to be justified, and favorable consideration is earnestly solicited.

Respectfully submitted,

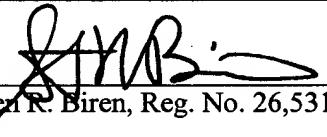
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